

Republic of the Philippines ILOILO SCIENCE AND TECHNOLOGY UNIVERSITY

La Paz, Iloilo City

• Trunkline: (033)320-7190 • Telefax: (033)329-4274 · Website: www.isatu.edu.ph



SUPPLEMENTAL / BID BULLETIN

November 8, 2021

ADDENDUM NO. 01

This supplemental/bid bulletin is being issued to further clarify the technical specifications of items for the **PROCUREMENT OF DIGITAL ELECTRONIC TRAINER BOARD FUND 164**.

Project Reference Number

ISAT U GOODS-2021-06-059

Location of the Contract

ISAT University Main Campus, Burgos Street, La Paz, Iloilo City

Fund Source

Fund 164

Approved Budget

PhP 200,000.00

Please be informed of the additional or corrected technical specifications of the items, as follow;

Digital Electronic Trainer Board - Corrected Technical Specifications

- ♣ 16 TTL/CMOS Logic Level Inputs with Dual Color LED for Logic Low & Logic High.
- 16 output LED's for Logic level Indicators.
- Fixed (TTL) Clock generator of 1Hz, 10Hz, 10Hz, 1KHz, 100KHz, 1MHz.
- Signal Generator Five step 200 Khz SINE, SQUARE(TTL), TRAINGLE output, Sine/Traingle Output Voltage - 20V p-p max.
- Dual Pulser Generator with four debounced Output Logic Probe to detect High/Low level pulses, with bi-colour LEDs to indicate Facility.
- Two digit 7 segment display with HEX to 7 segment decoder.
- Two digit 7 segment display with all segment inputs
- LED BAR graph with 10 LED indicators to display 0-5 V input.
- On board DPM (4 no) provided with mode selection: DC volt/ current.
- On-board 1K & 1M Variable Potentiometer.
- On-board Buzzer for alarm application.
- On-board +12V SPDT Relay for Control application.
- On-board 1280 TIE points Bread Board.
- ±12V/250mA. Fixed DC Power Supply: +5V/2A,
- Variable DC Power supply of 0 to +15V, 0 to -15V &0 to +30V output.
- C Power Supply of 15V-0-15V.
- All Inputs/Outputs are brought on 2mm Sockets
- Set of 2mm Banana PatchCords.
- Should support KMS series ready to use Electronics board.
- Bare board Tested Glass Epoxy SMOBC PCB is used.
- User's Manual.

Digital experimental boards:

CATEC/ADITHMATTC LOGIC BOARD

(SE)

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- DN-03 BUFFER/LATCH/ SEVEN SEGMENT DECODER BOARD
 - Experiments on Buffer output.
 - Experiments on Latch output.
 - Experiments on Seven Segment Decoder.
- 4. DN-04 FLIP FLOP/ SHIFT REGISTER BOARD
 - Experiments on RS, T, & D Flip Flop.
 - Experiments on JK Flip Flop & Master Slave JK Flip Flop.
 - Experiments on Universal Shift Register.
- 5. DN-05 MULTIPLEXER/DEMUX/ MAGNITUDE COMPARATOR BOARD.
 - Experiments on 8 channel Multiplexer.
 - Experiments on 8 channel Demultiplexer.
 - Experiments on 4 bit Magnitude Comparator.
- DN-06 SYNCHRONOUS/ ASYNCHRO-NOYS COUNTER BOARD.
 - Experiments on 4 bit Asynchronous Counter.
 - Experiments on 4 bit Synchronous Counter.
- DN-06 8 BIT ADC & DAC BOARD.
 - Experiments on 8 bit Analog to Digital Convertor.
 - Experiments on 8 bit Digital to Analog Convertor.
- 8. DN-08 EPROM/RAM EXPERIMENTAL BOARD
 - Experiments on Program & Write operation of 64k Eprom.
 - Experiments on Read & Write operation of 32K RAM.
- DN-09 CPLD XC9572 BOARD.
 - Experiments on Full Adder, Adder/ Substractor.
 - Experiments on Seven Segment Decoder.
 - Experiments on Binary to Grey Conversion.
 - Experiments on Comparator, Decoder, Demultiplexer.
 - Experiments on Encoder, Multiplexer, Parity Generator.
 - Experiments on T, D JK Flip Flop

This Supplemental Bid Bulletin No. 1 shall form part of the Bidding Documents. For the guidance and information of all concerned.

DR. CORAZON C. CORBAL BAC Chair